IBIS/HSPICE Model Quality Report

Design ID: T69M
Description: 2Gb (128Mb x16, 64Mb x32) Mobile LPDDR SDRAM
Marketing device name(s): MT46H128M16LFCK, MT46H64M32LFCM, MT46H64M32LFMA, MT46H64M32LFMB, MT46H128M16LFT69M, MT46H64M32LFT69M, MT46H128M32L2KQ, MT46H256M32L4JV, MT46H128M32L2CA, MT46H256M32L4KZ, MT46H128M32L2MC, MT46HC128M16LFCK, MT46HC64M32LFCM, MT46HC128M16LFT69M, MT46HC64M32LFT69M[1]
Valid Speed Grades: DDR-400, DDR-370, DDR-333, DDR-266
Zip File Name: t69m_ibis.zip
IBIS File name: t69m.ibs, t69m_it.ibs, t69m_at.ibs **File rev:** 1.0
HSPICE File name: t69m_hspice.zip **File rev:** 1.0
EBD file name: t69m_168b_2dp.ebd, t69m_168b_4dp.ebd **File rev:** 1.1
EBD file name: t69m_152b_2dp.ebd, t69m_152b_4dp.ebd, t69m_240b_2dp.ebd **File rev:** 1.0
Die Rev: A
Date: February 15, 2010
Datasheet Link:

E-mail at modelsupport@micron.com for questions regarding Quality Report

Device Parameters

VDDQ – Slow: 1.7V **Typical:** 1.8V **Fast:** 1.95V
VDDQ – Slow: 1.14V **Typical:** 1.2V **Fast:** 1.3V
VDD – Slow: 1.7V **Typical:** 1.8V **Fast:** 1.95V
Junction Temperature (Commercial) - Slow: 85C **Typical:** 50C **Fast:** 0C
Junction Temperature (Industrial) - Slow: 100C **Typical:** 50C **Fast:** -40C
Junction Temperature (Automotive) - Slow: 120C **Typical:** 50C **Fast:** -40C
VDDQ/VSSQ Decoupling Capacitance: 1.16nF
Included in HSPICE DQ/DQS models? Yes **Amount per DQ/DQS model:** 39.4pF
VDDQ/VSSQ Decoupling Capacitance Series Resistance: See t69m_model.cnr for details

IBIS Quality Summary

1. ☒ Include the IBIS Quality Summary information in the Quality report. For details on IBIS Quality check the quality specification and quality checklist on IBIS quality webpage http://www.vhdl.org/pub/ibis/quality_wip/

|##
IBIS Quality Notes

```
|################################################################
|IQ SUMMARY Overall Quality of component and models Level 2b
|
|IQ Level 0 - 0 errors 0 warnings
|IQ Level 1 - All checks done for completeness and correctness
|IQ Level 2 - HSPICE Correlation
|IQ Buffer DQ_FULL_18/DQ_FULL_12: Quality level 2b
|IQ Buffer DQ_HALF_18/DQ_HALF_12: Quality level 2b
|IQ Buffer DQ_QTR_18/DQ_QTR_12: Quality level 2b
|IQ Buffer DQ_3QTR_18/DQ_3QTR_12: Quality level 2b
|IQ Buffer DM_INPUT_18/DM_INPUT_12: Quality level 2b
|IQ Buffer CLK_INPUT_18/CLK_INPUT_12: Quality level 2b
|IQ Buffer INPUT_18/INPUT_12: Quality level 2b
|
|IQ Level 1
|   All Level 1 checks performed and are either OK or NA
|
|IQ Level 2
|   Using VT IBIS Data compared to source hspice models
|
|IQ Level 2b
|   C_comp hspice correlation
|
|IQ BEGIN IBIS Quality Checklist
|IQ FILE: t69m.ibs, t69m_it.ibs, t69m_at.ibs        IQ Level:    1
|IQ COMPONENT: MT46H128M16LFCK                      IQ Level:    1
|IQ COMPONENT: MT46H64M32LFCM                       IQ Level:    1
|IQ COMPONENT: MT46H64M32LFMA                       IQ Level:    1
|IQ COMPONENT: MT46H64M32LFMB                       IQ Level:    1
|IQ COMPONENT: MT46H128M16LFT69M_DS                 IQ Level:    1
|IQ COMPONENT: MT46H64M32LFT69M_DS                  IQ Level:    1
|IQ COMPONENT: MT46H128M16LFT69M_SS                 IQ Level:    1
|IQ COMPONENT: MT46H64M32LFT69M_SS                  IQ Level:    1
|IQ COMPONENT: MT46HC128M16LFCK                     IQ Level:    1
|IQ COMPONENT: MT46HC64M32LFCM                      IQ Level:    1
|IQ COMPONENT: MT46HC128M16LFT69M_DSIQ Level:    1
|IQ COMPONENT: MT46HC64M32LFT69M_DS                 IQ Level:    1
|IQ COMPONENT: MT46HC128M16LFT69M_SS                IQ Level:    1
|IQ COMPONENT: MT46HC64M32LFT69M_SS                 IQ Level:    1
|IQ MODEL: DQ_FULL_18                               IQ Level:    2b
|IQ MODEL: DQ_FULL_12                               IQ Level:    2b
|IQ MODEL: DQ_HALF_18                               IQ Level:    2b
|IQ MODEL: DQ_HALF_12                               IQ Level:    2b
```


|IQ MODEL: DQ_QTR_18	IQ Level:	2b
|IQ MODEL: DQ_QTR_12	IQ Level:	2b
|IQ MODEL: DQ_3QTR_18	IQ Level:	2b
|IQ MODEL: DQ_3QTR_12	IQ Level:	2b
|IQ MODEL: INPUT_18	IQ Level:	2b
|IQ MODEL: INPUT_12	IQ Level:	2b
|IQ MODEL: DM_INPUT_18	IQ Level:	2b
|IQ MODEL: DM_INPUT_12	IQ Level:	2b
|IQ MODEL: CLK_INPUT_18	IQ Level:	2b
|IQ MODEL: CLK_INPUT_12	IQ Level:	2b
|IQ END IBIS Quality Checklist		

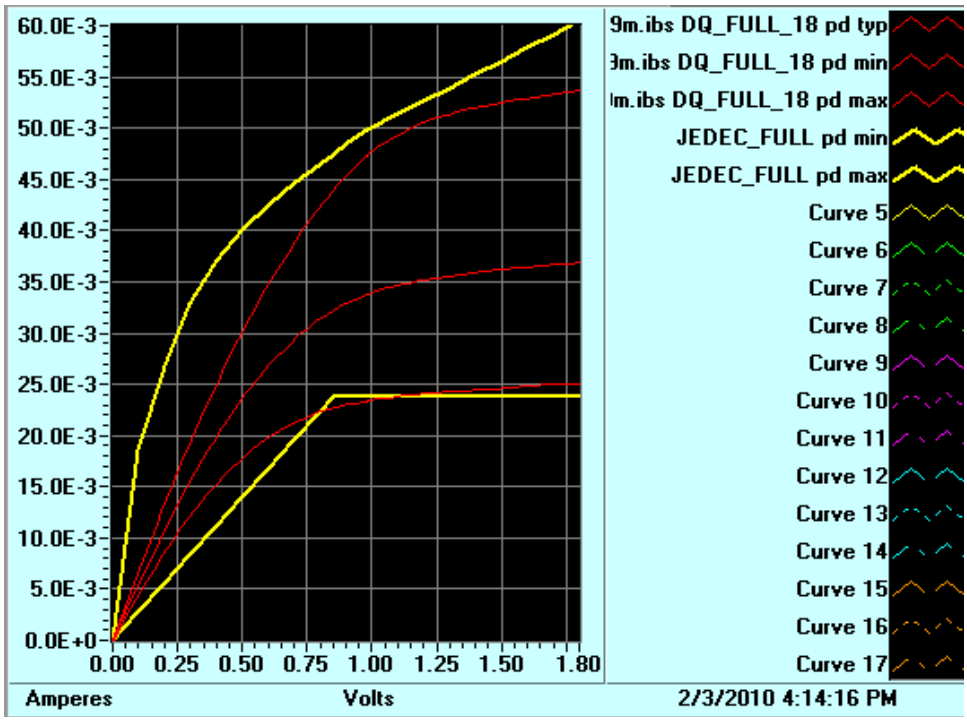
IBIS MODEL Correlation

Datasheet Correlation

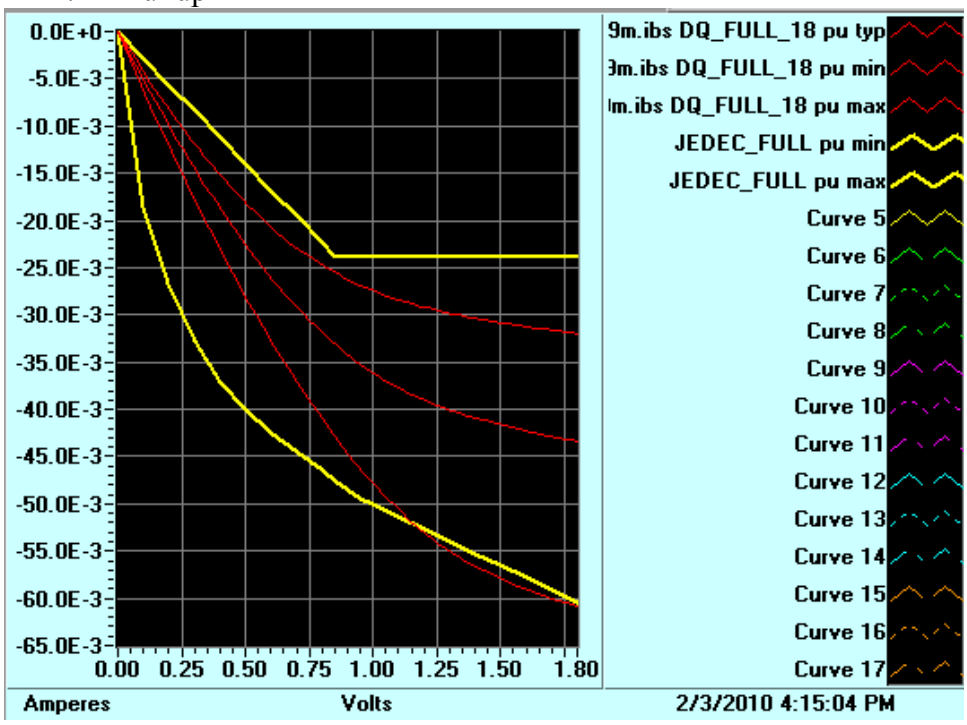
1. ☒ For Output model or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

a. Model Name **DQ_FULL_18**

i. Pulldown

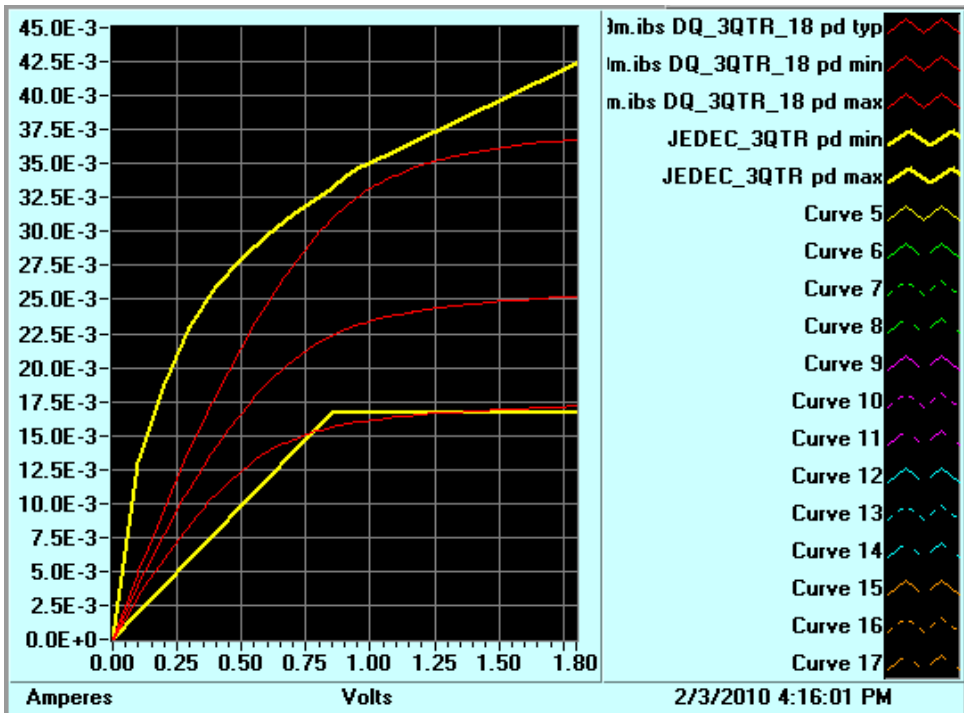


ii. Pullup

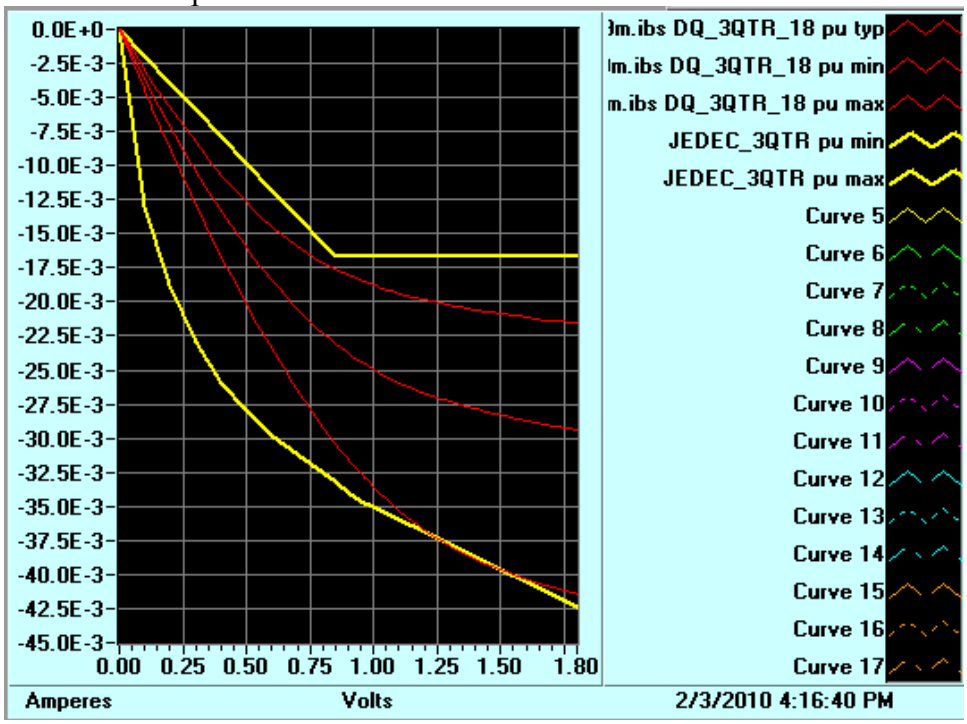


b. Model Name **DQ_3QTR_18**

i. Pulldown

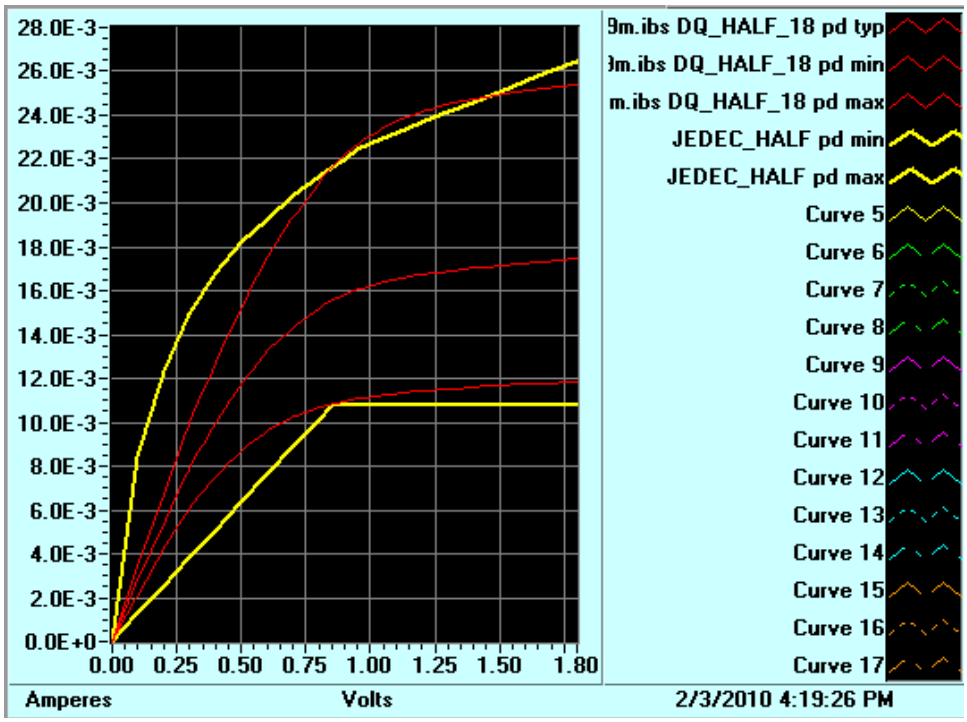


ii. Pullup

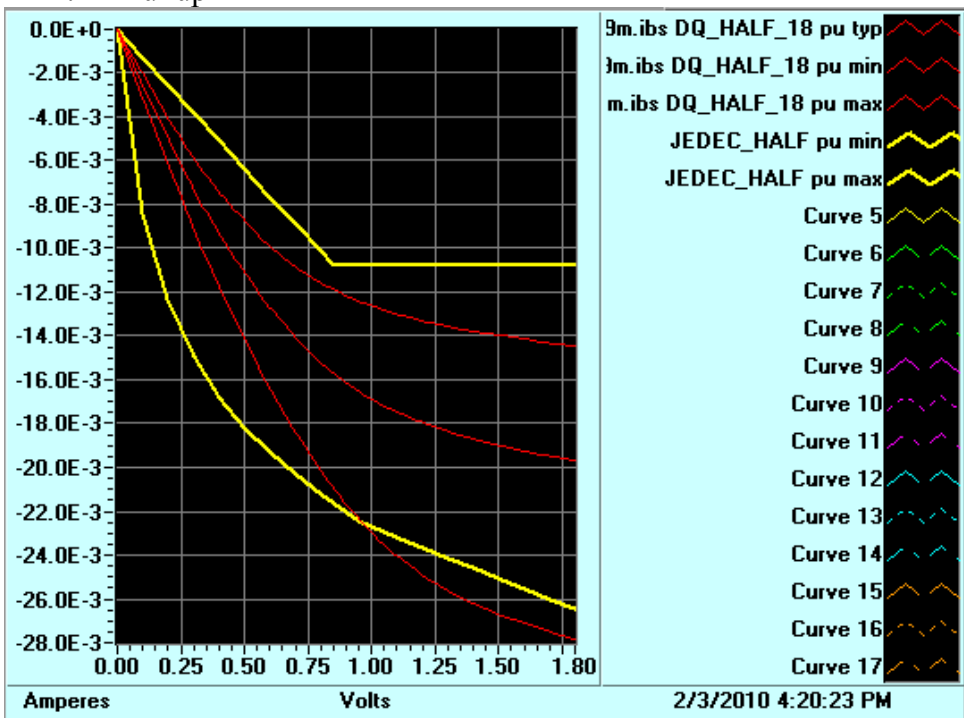


c. Model Name **DQ_HALF_18**

i. Pulldown

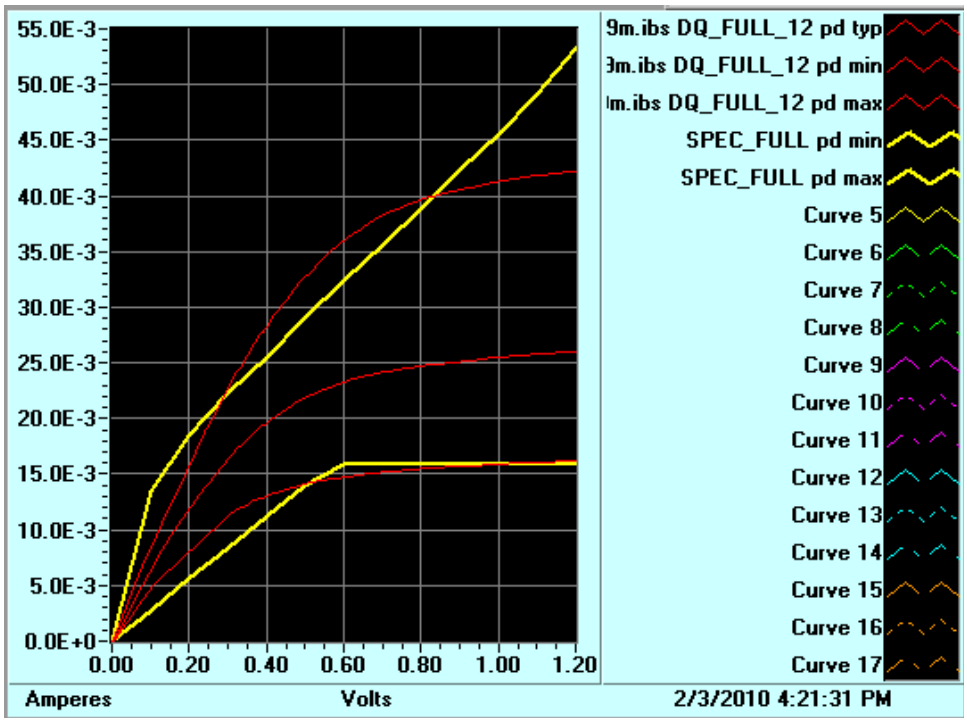


ii. Pullup

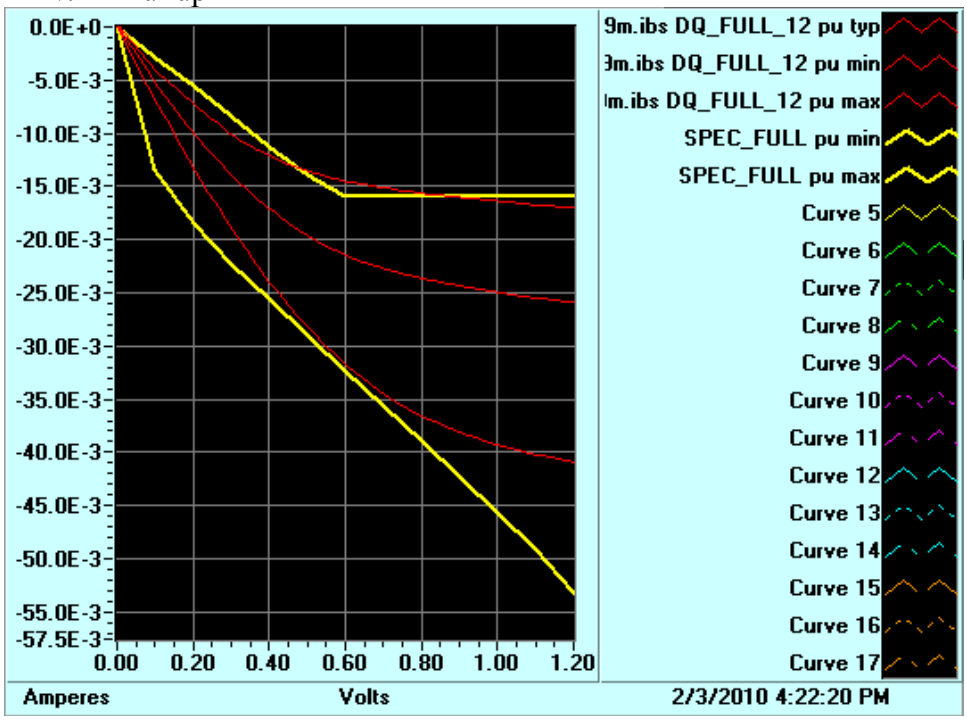


d. Model Name **DQ_FULL_12**

iii. Pulldown

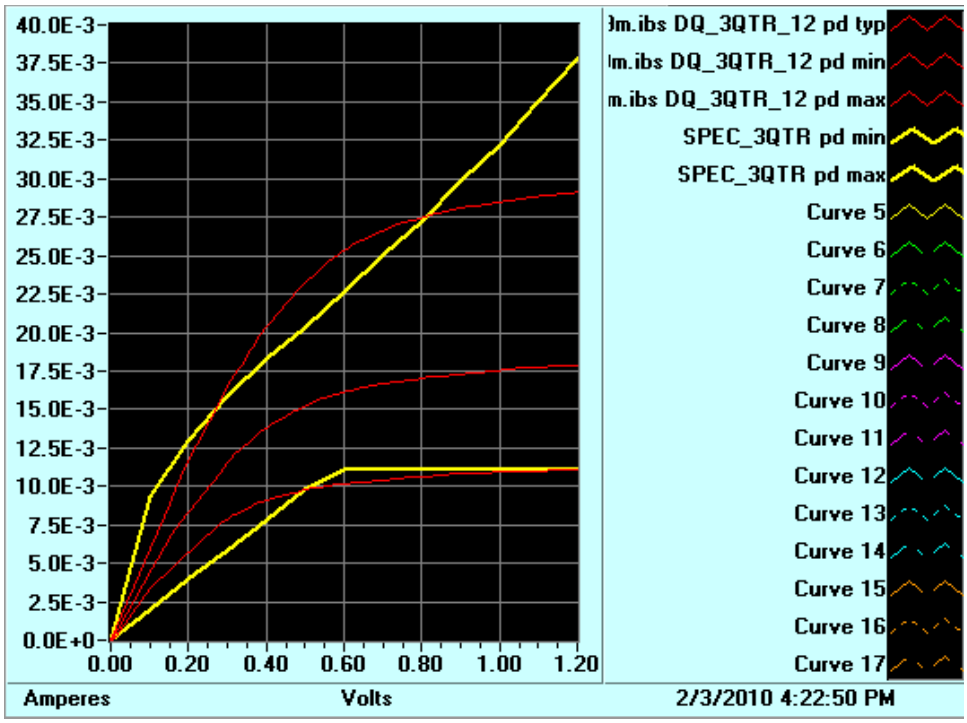


iv. Pullup

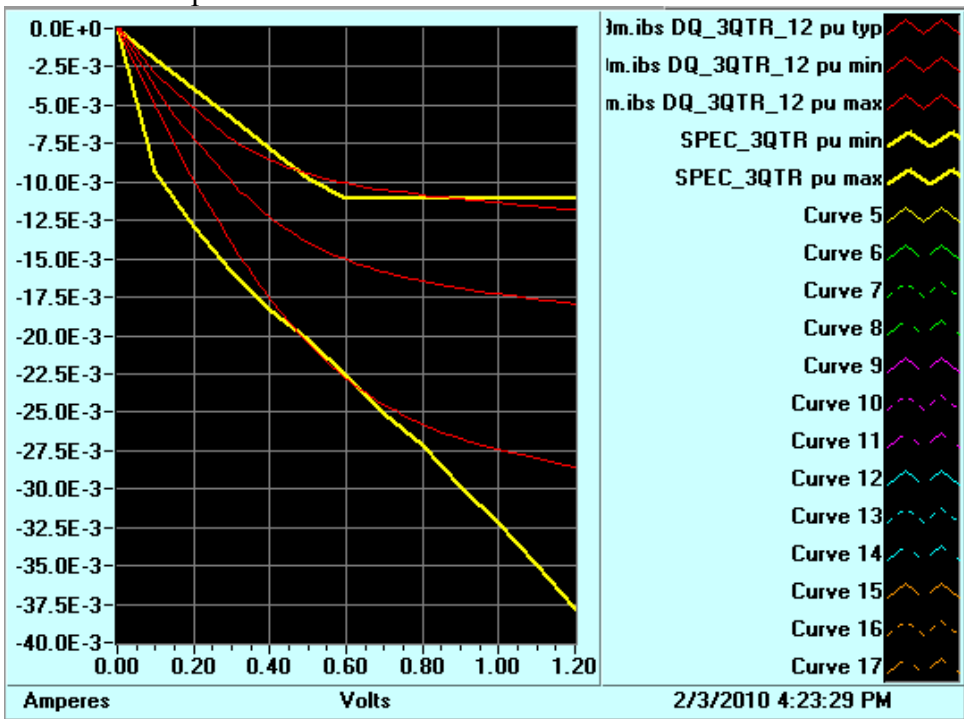


e. Model Name **DQ_3QTR_12**

iii. Pulldown

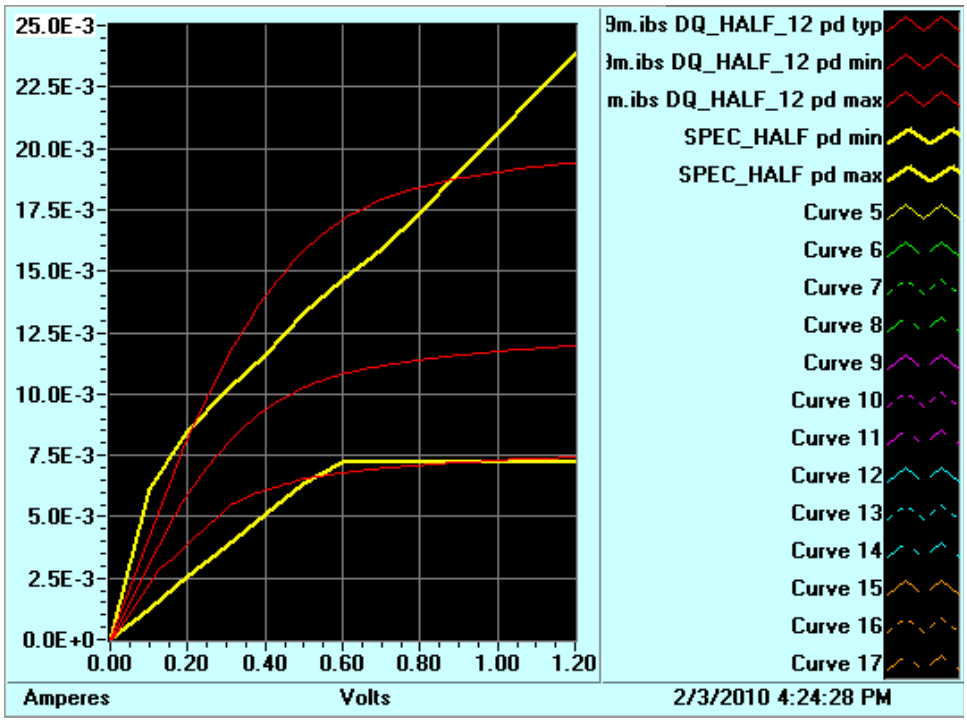


iv. Pullup

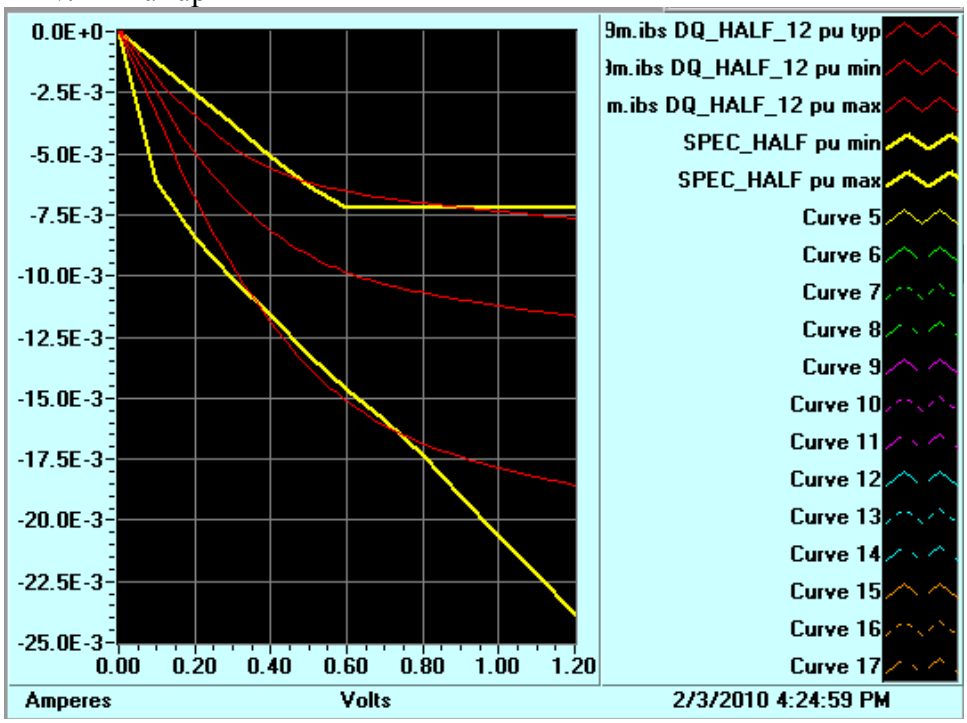


f. Model Name **DQ_HALF_12**

iii. Pulldown



iv. Pullup



2. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16)[2]

Insert component name here **MT46H64M32LFCM, MT46HC64M32LFCM (90-Ball VFBGA)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	1.54	1.69	NA	NA
	C package	1.48	1.90	NA	NA
	C_total	3.02	3.59	2.0	4.5
INPUT	C_comp	1.33	1.48	NA	NA
	C package	1.36	1.79	NA	NA
	C_total	2.70	3.27	1.5	3.0
CLK	C_comp	1.33	1.48	NA	NA
	C package	1.65	1.89	NA	NA
	C_total	2.98	3.37	1.5	3.0

Insert component name here **MT46H128M16LFCK, MT46HC128M16LFCK (60-Ball VFBGA)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	1.54	1.69	NA	NA
	C package	1.65	1.93	NA	NA
	C_total	3.19	3.63	2.0	4.5
INPUT	C_comp	1.18	1.48	NA	NA
	C package	1.44	1.89	NA	NA
	C_total	2.63	3.37	1.5	3.0
CLK	C_comp	1.18	1.48	NA	NA
	C package	1.40	1.53	NA	NA
	C_total	2.59	3.02	1.5	3.0

Insert component name here **MT46H64M32LFMA (168-Ball OMAP PoP)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	1.54	1.69	NA	NA
	C package	0.65	1.39	NA	NA
	C_total	2.19	3.08	2.0	4.5
INPUT	C_comp	1.33	1.48	NA	NA
	C package	0.83	1.78	NA	NA
	C_total	2.17	3.26	1.5	3.0
CLK	C_comp	1.33	1.48	NA	NA
	C package	0.65	0.76	NA	NA
	C_total	1.99	2.24	1.5	3.0

Insert component name here **MT46H64M32LFMB (152-Ball OMAP PoP)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	1.54	1.69	NA	NA
	C package	0.63	1.18	NA	NA
	C_total	2.17	2.87	2.0	4.5
INPUT	C_comp	1.33	1.48	NA	NA
	C package	1.00	1.98	NA	NA
	C_total	2.34	3.46	1.5	3.0
CLK	C_comp	1.33	1.48	NA	NA
	C package	0.73	0.76	NA	NA
	C_total	2.06	2.24	1.5	3.0

3. ☐ If slew rate specifications (Rise slew and Fall slew) are available from the datasheet, complete HSPICE simulation to generate slew rate data and provide a comparison table.

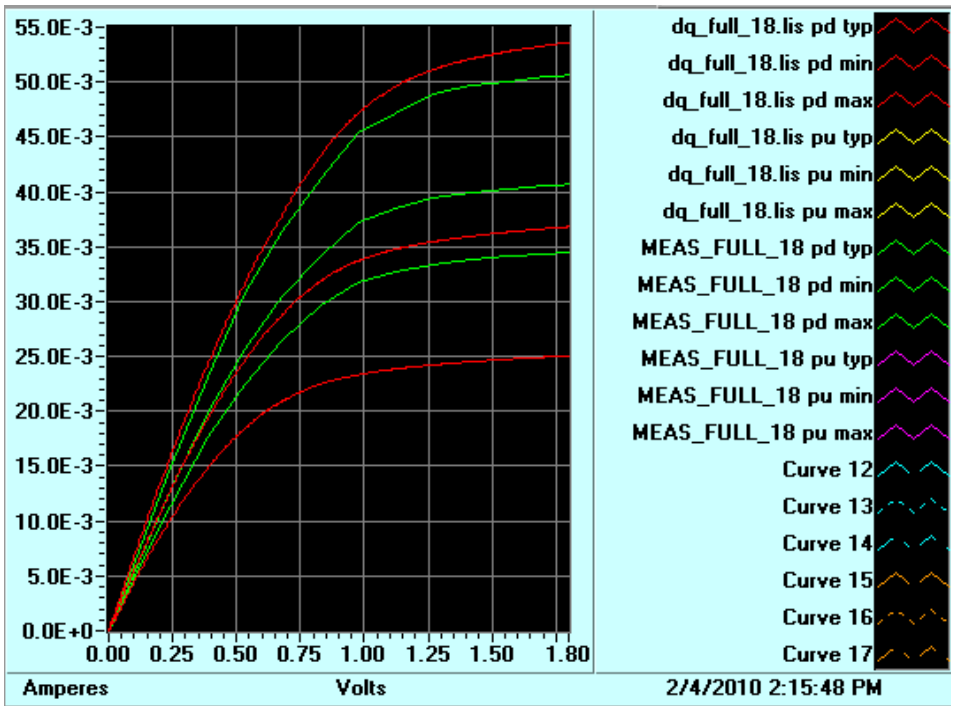
   Not available

Measurement Correlation

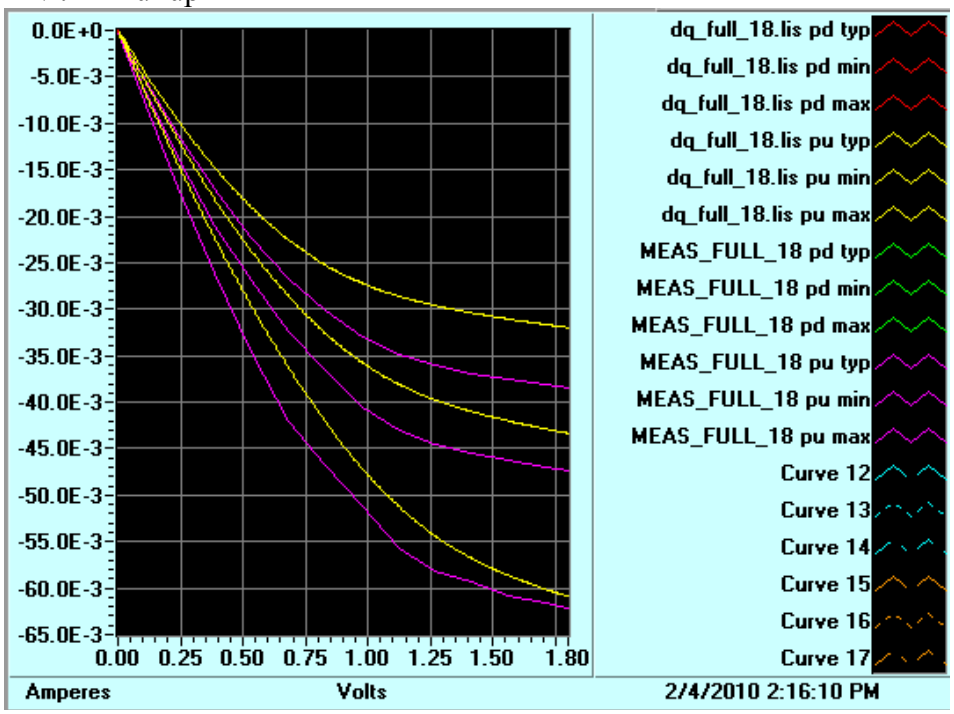
1. ☒ For Output model or I/O model compare measured IOH/IOL data with IBIS pullup pulldown data. If the measurement condition is different than IBIS condition, run hspice simulation using the same measurement condition, for example Vcc, temp and process. Include measurement conditions in the pullup/pulldown images.

a. Model Name **DQ_FULL_18 (Typ=TT, 1.8V, 25C; Min=SS, 1.7V, 85C; Max=FF, 1.95V, -40C)**

v. Pulldown

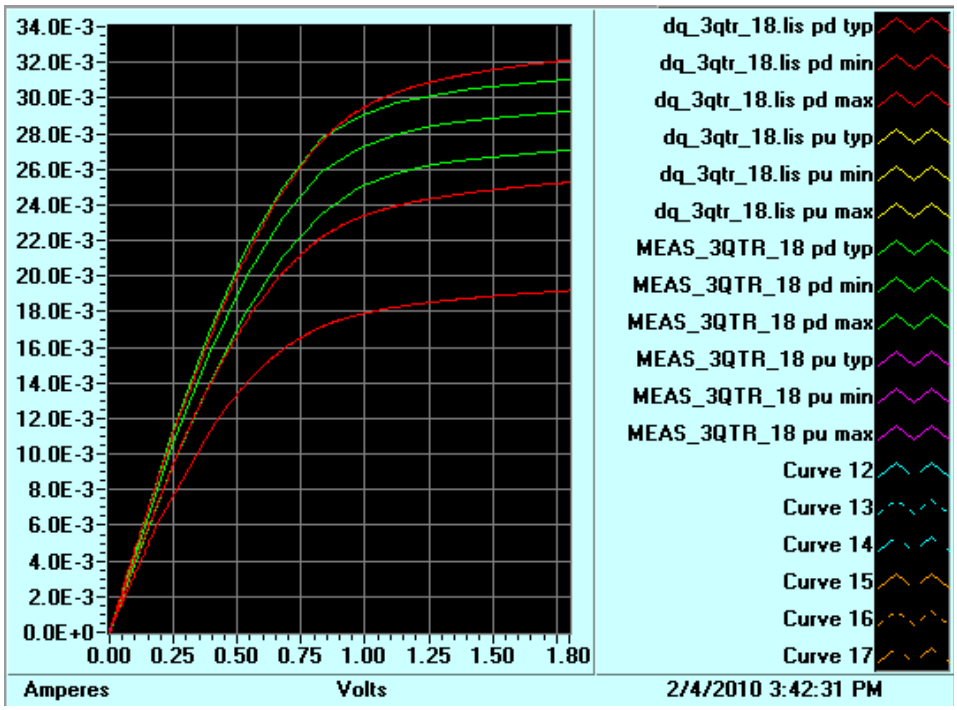


vi. Pullup

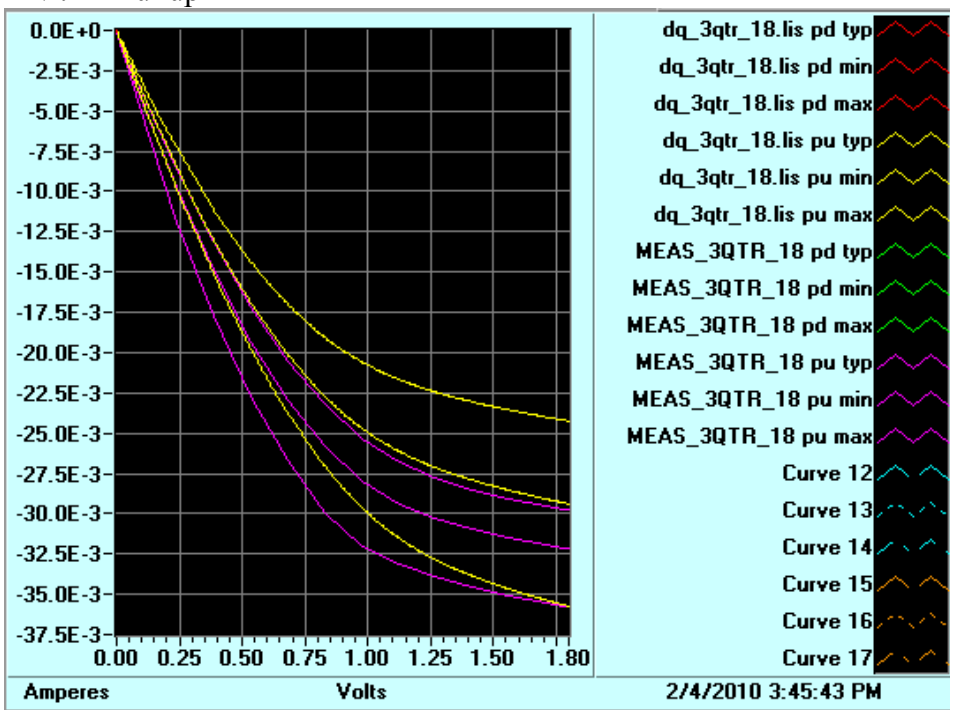


b. Model Name **DQ_3QTR_18 (Typ=TT, 1.8V, 25C; Min=SS, 1.8V, 85C; Max=FF, 1.8V, -40C)**

v. Pulldown

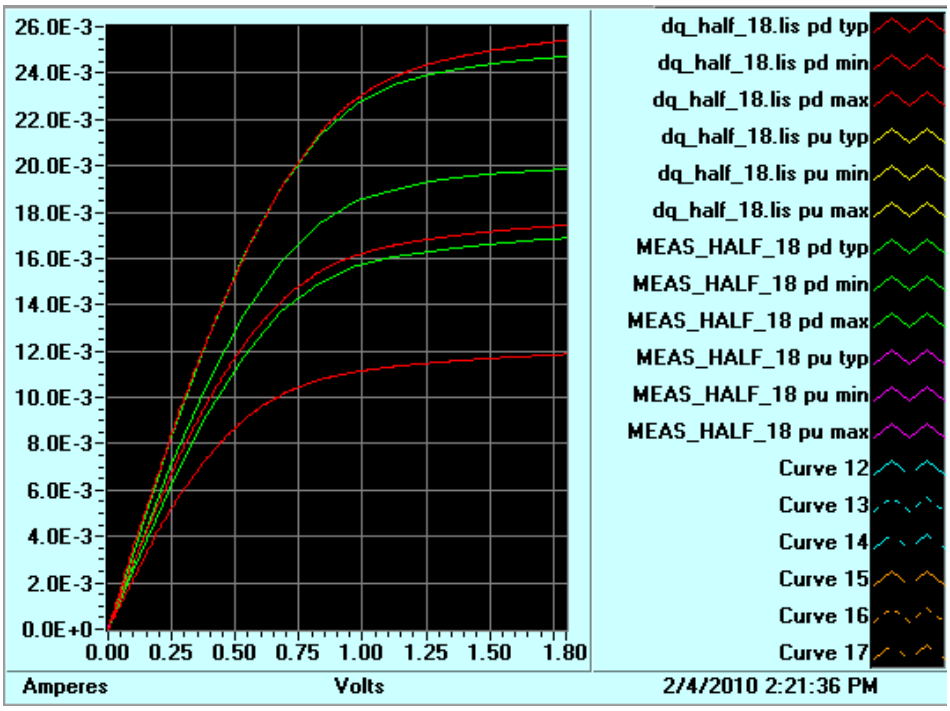


vi. Pullup

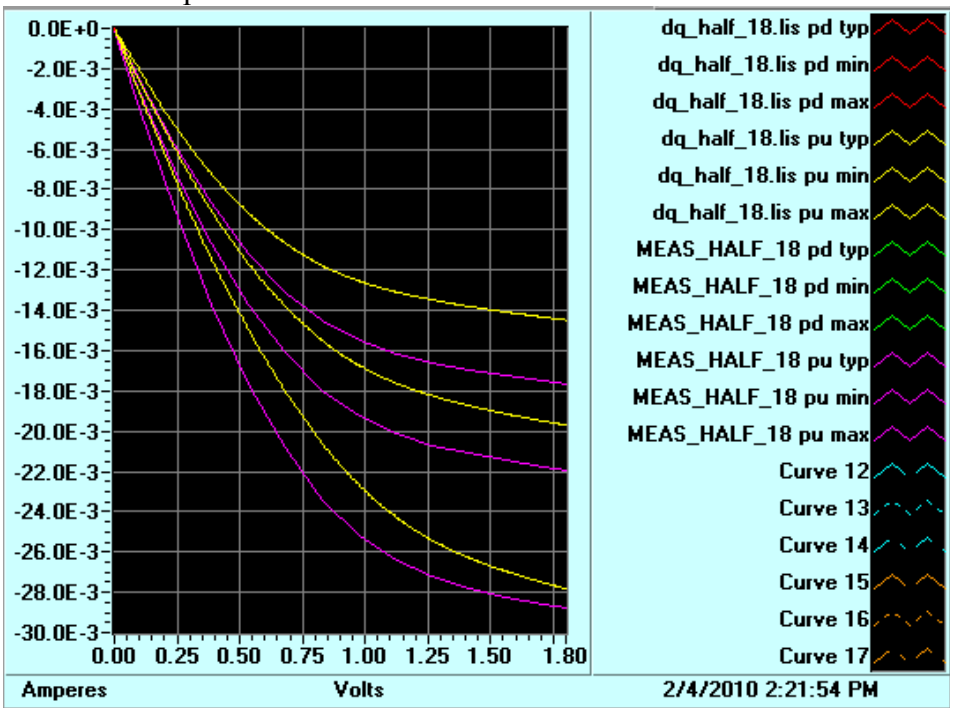


c. Model Name **DQ_HALF_18 (Typ=TT, 1.8V, 25C; Min=SS, 1.7V, 85C; Max=FF, 1.95V, -40C)**

v. Pulldown

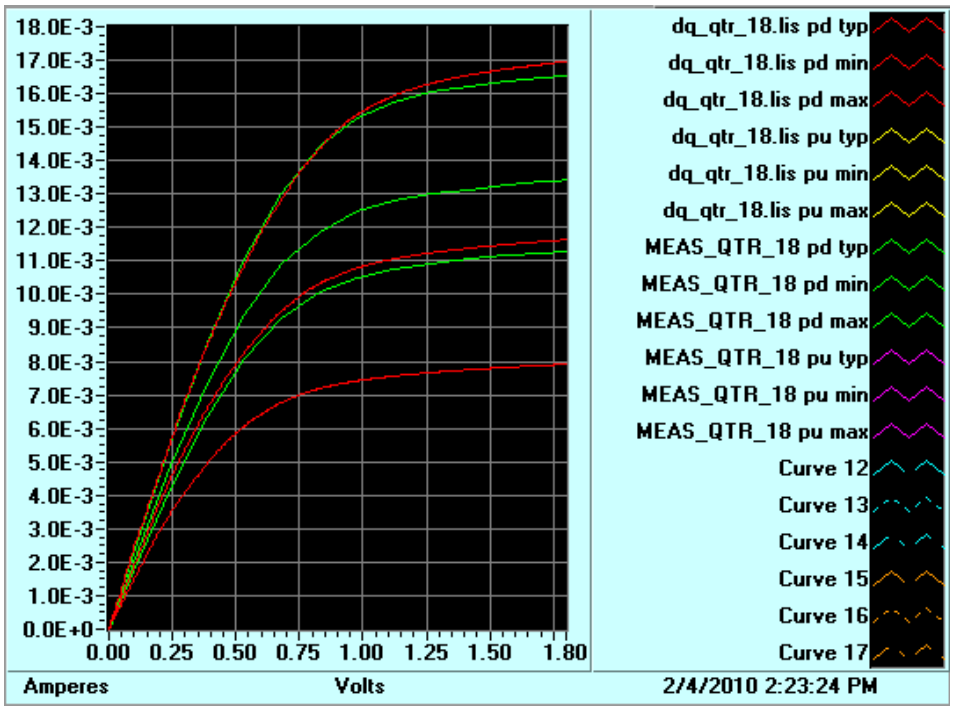


vi. Pullup

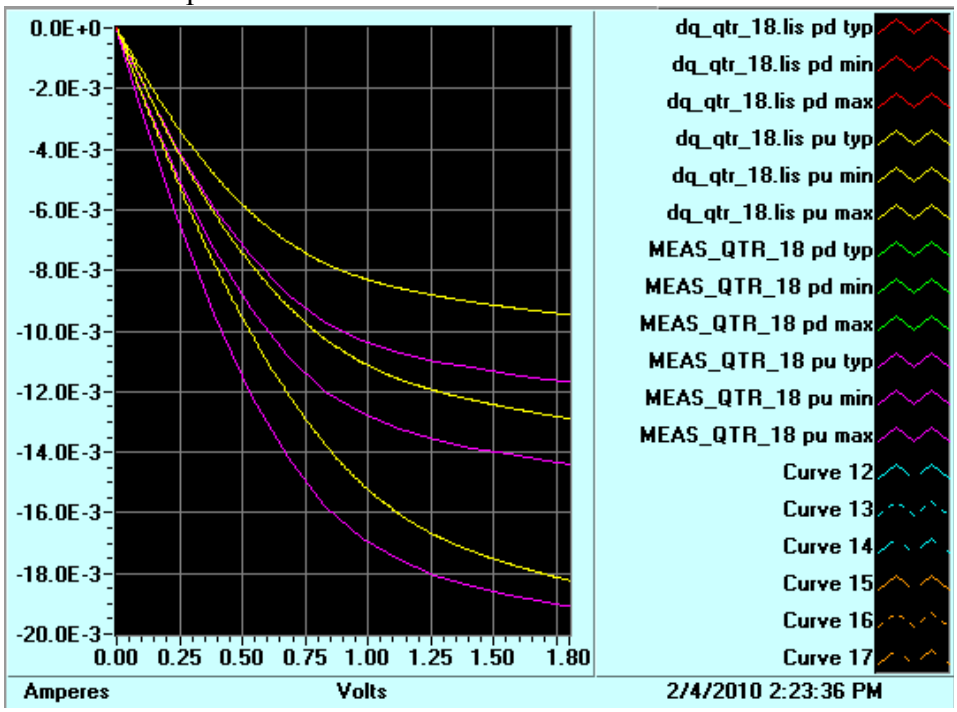


d. Model Name **DQ_QTR_18 (Typ=TT, 1.8V, 25C; Min=SS, 1.7V, 85C; Max=FF, 1.95V, -40C)**

vii. Pulldown

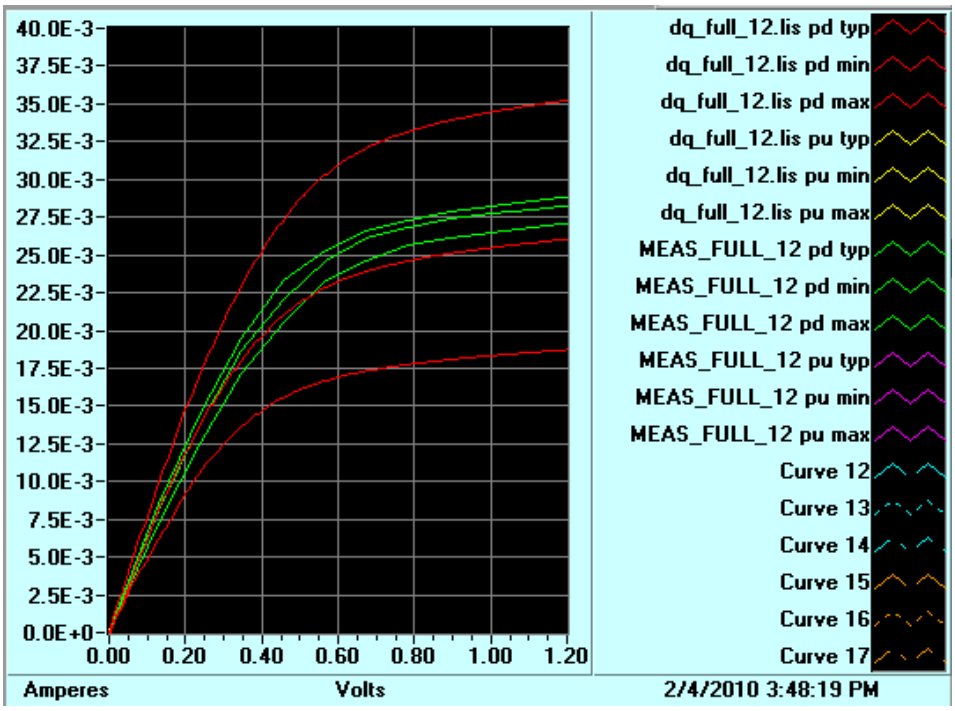


viii. Pullup

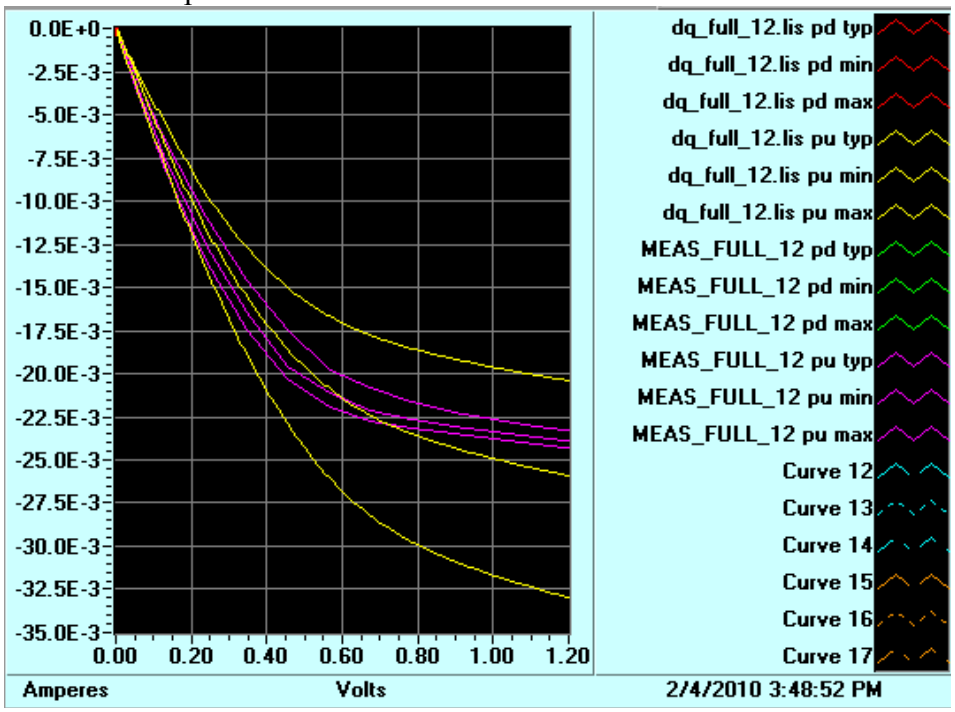


e. Model Name **DQ_FULL_12 (Typ=TT, 1.2V, 25C; Min=SS, 1.2V, 90C; Max=FF, 1.2V, -40C)**

vii. Pulldown

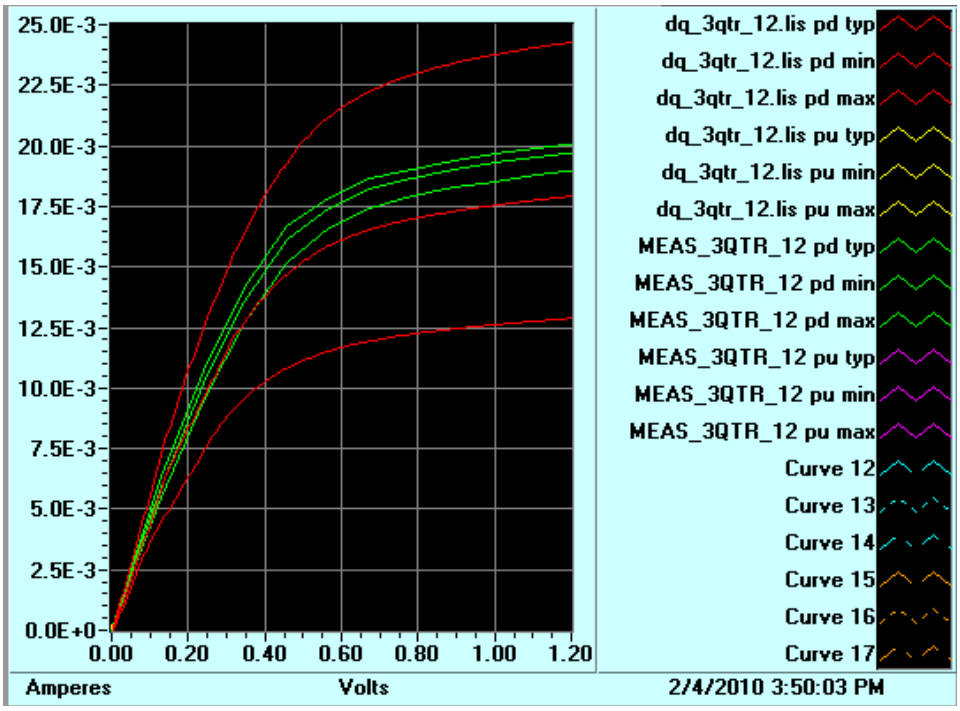


viii. Pullup

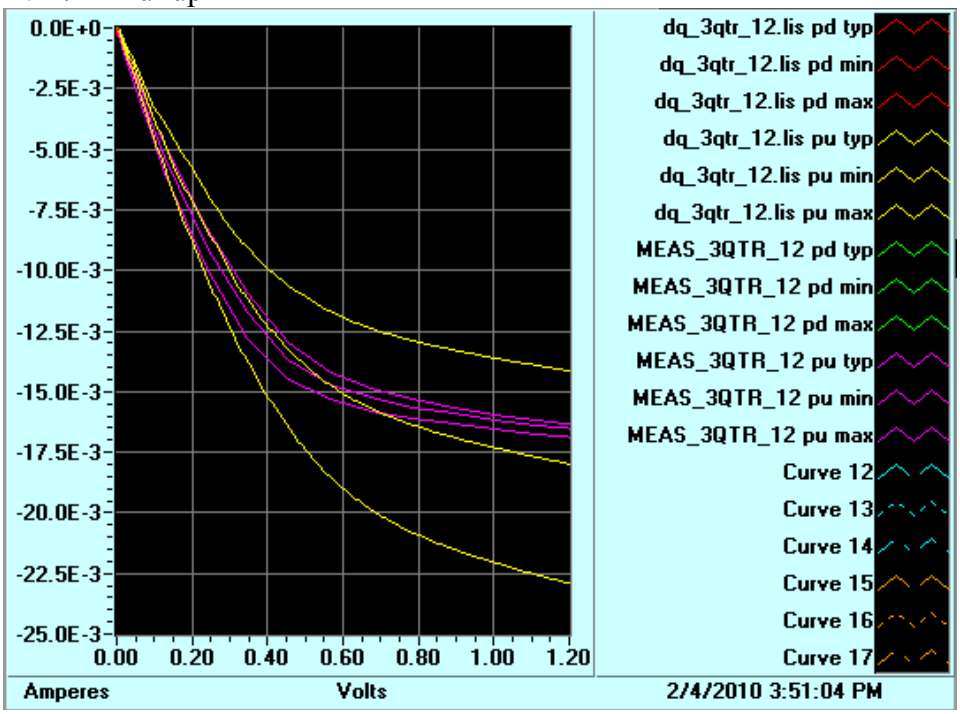


f. Model Name **DQ_3QTR_12 (Typ=TT, 1.2V, 25C; Min=SS, 1.2V, 90C; Max=FF, 1.2V, -40C)**

vii. Pulldown

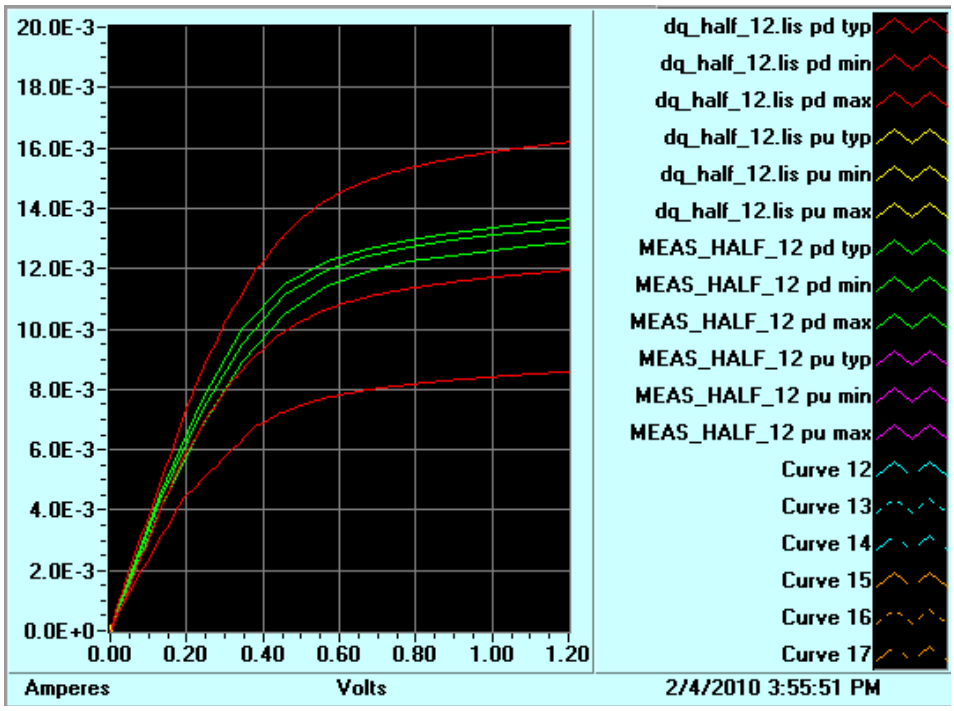


viii. Pullup

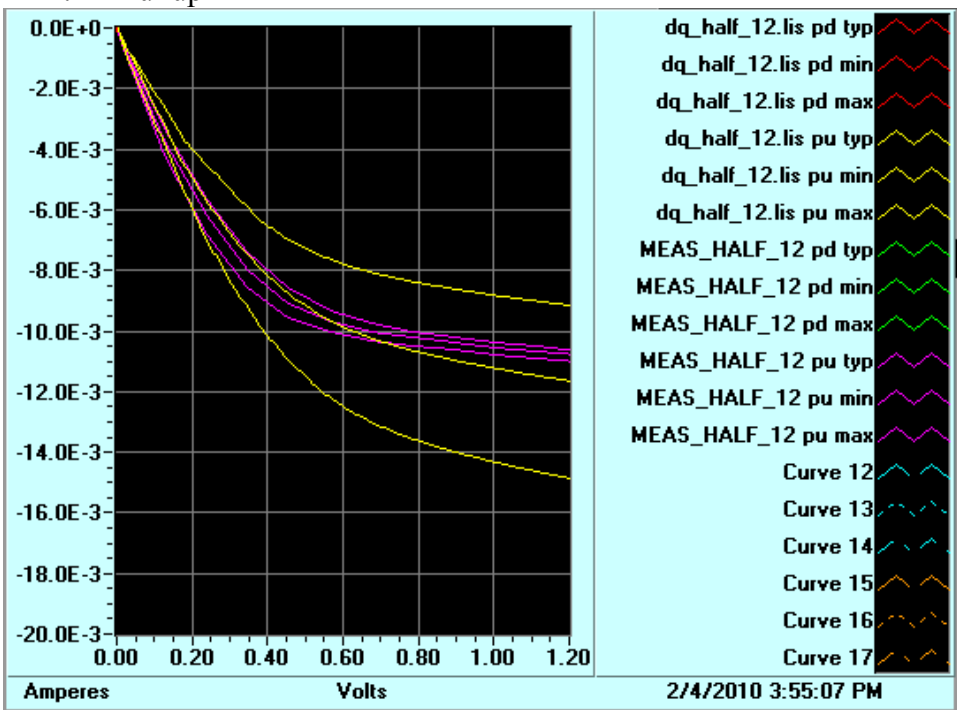


g. Model Name **DQ_HALF_12 (Typ=TT, 1.2V, 25C; Min=SS, 1.2V, 90C; Max=FF, 1.2V, -40C)**

ix. Pulldown

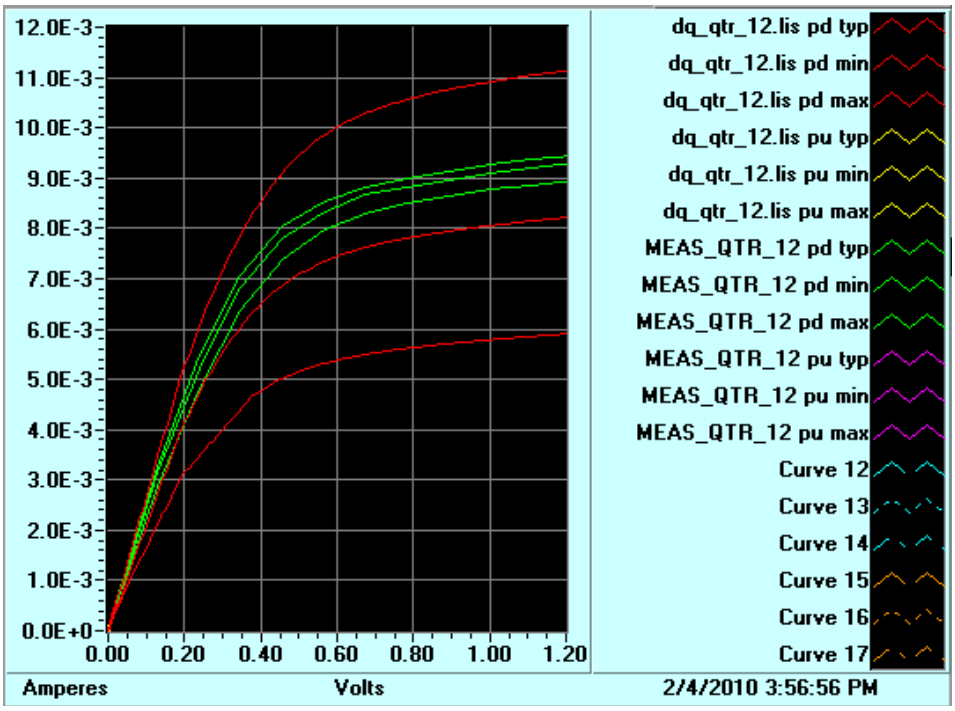


x. Pullup

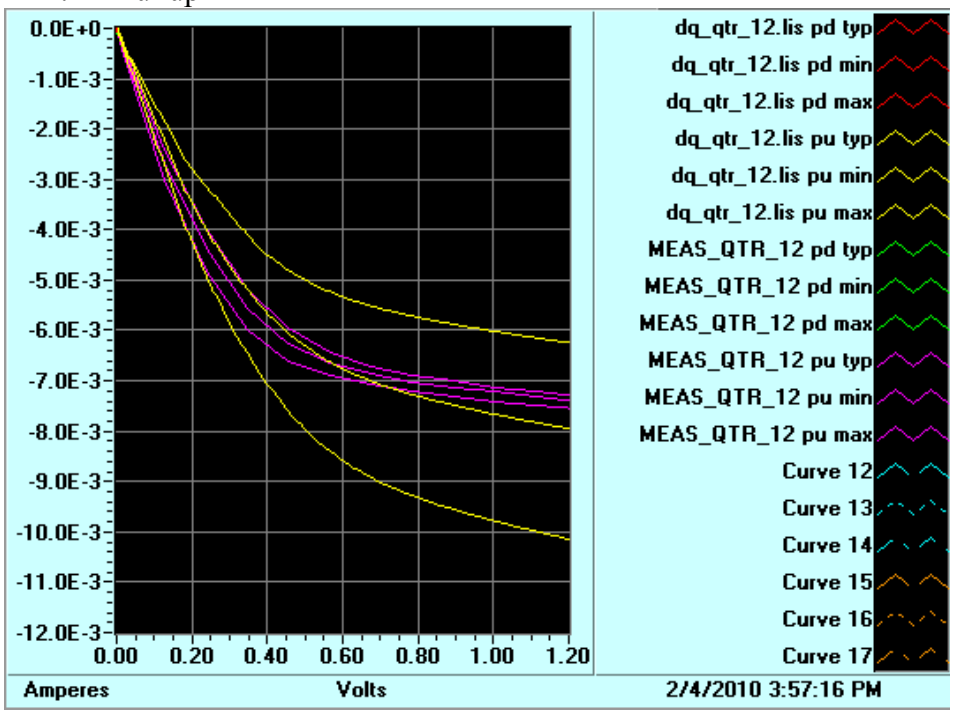


h. Model Name **DQ_QTR_12 (Typ=TT, 1.2V, 25C; Min=SS, 1.2V, 90C; Max=FF, 1.2V, -40C)**

ix. Pulldown



x. Pullup



2. ☒ Compare C_comp with measured C_comp. Provide C_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16)

Insert component name here **MT46H64M32LFCM, MT46HC64M32LFCM (90-Ball VFBGA)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	1.54	1.39	1.69	NA	NA	NA
	C package	1.48	1.63	1.90	NA	NA	NA
	C_total	3.02	3.02	3.59	2.90	3.16	3.44
INPUT	C_comp	1.33	1.18	1.48	NA	NA	NA
	C package	1.36	1.58	1.79	NA	NA	NA
	C_total	2.70	2.76	3.27	2.60	2.94	3.20
CLK	C_comp	1.33	1.18	1.48	NA	NA	NA
	C package	1.65	1.77	1.89	NA	NA	NA
	C_total	2.98	2.95	3.37	2.88	2.97	3.06

Insert component name here **MT46H128M16LFCK, MT46HC128M16LFCK (60-Ball VFBGA)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	1.54	1.39	1.69	NA	NA	NA
	C package	1.65	1.74	1.93	NA	NA	NA
	C_total	3.19	3.13	3.63	3.16	3.28	3.45
INPUT	C_comp	1.18	1.33	1.48	NA	NA	NA
	C package	1.44	1.65	1.89	NA	NA	NA
	C_total	2.63	2.98	3.37	2.79	3.01	3.22
CLK	C_comp	1.18	1.33	1.48	NA	NA	NA
	C package	1.40	1.47	1.53	NA	NA	NA
	C_total	2.59	2.80	3.02	2.68	2.74	2.81

Insert component name here **MT46H64M32LFMA (168-Ball OMAP PoP)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	1.54	1.39	1.69	NA	NA	NA
	C package	0.65	1.10	1.39	NA	NA	NA
	C_total	2.19	2.49	3.08	2.21	2.52	2.89
INPUT	C_comp	1.33	1.18	1.48	NA	NA	NA
	C package	0.83	1.31	1.78	NA	NA	NA
	C_total	2.17	2.49	3.26	2.18	2.60	3.08
CLK	C_comp	1.33	1.18	1.48	NA	NA	NA
	C package	0.65	0.71	0.76	NA	NA	NA
	C_total	1.99	1.89	2.24	1.97	2.03	2.10

3. ☐ If measured clamp current data is available provide an IBIS and Silicon clamp comparison for all models

   Not available

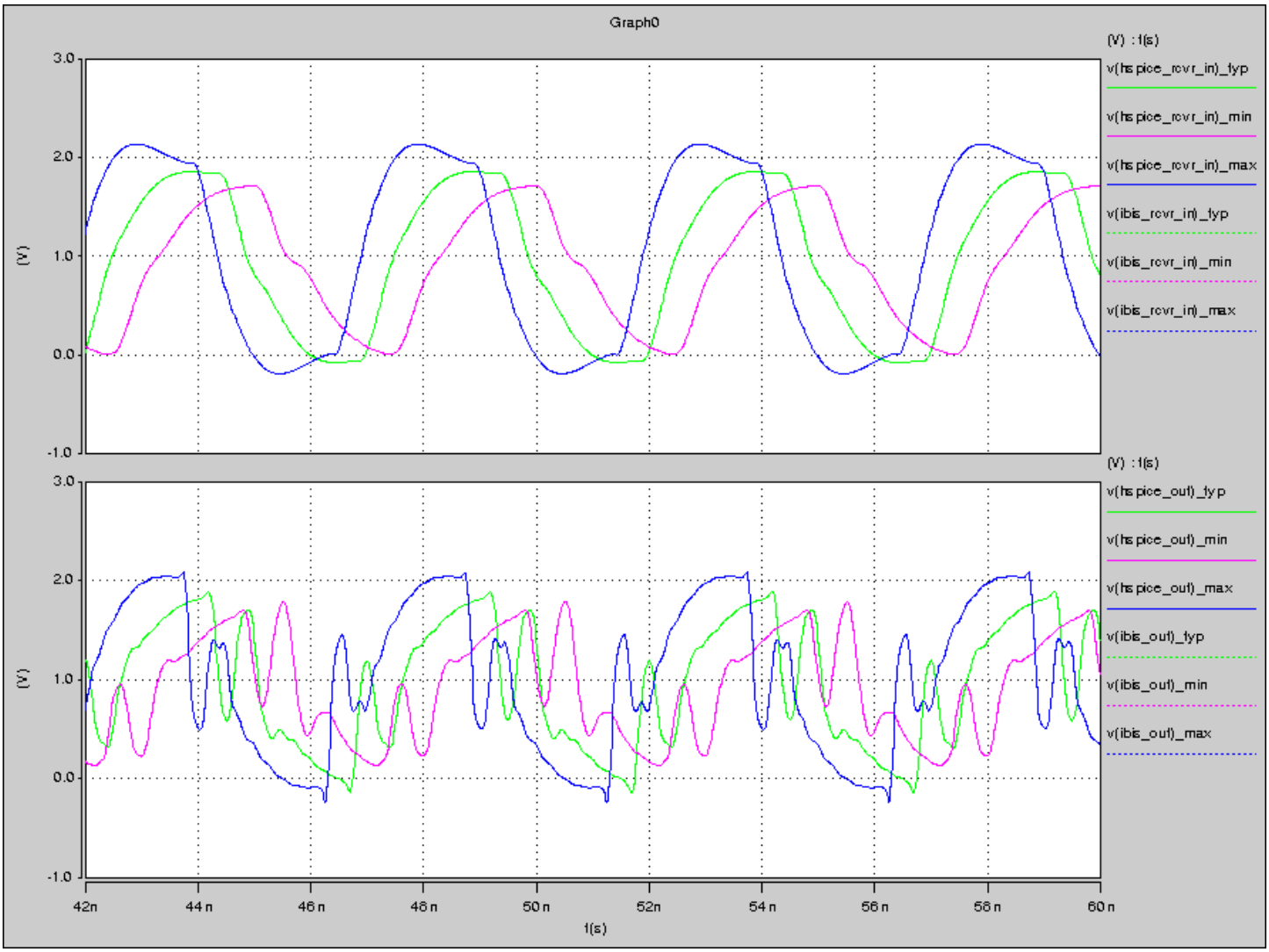
4. ☐ If slew rate specifications (Rise slew and Fall slew) are available from measurements, complete HSPICE simulation to generate slew rate data and provide a comparison table.

   Not available

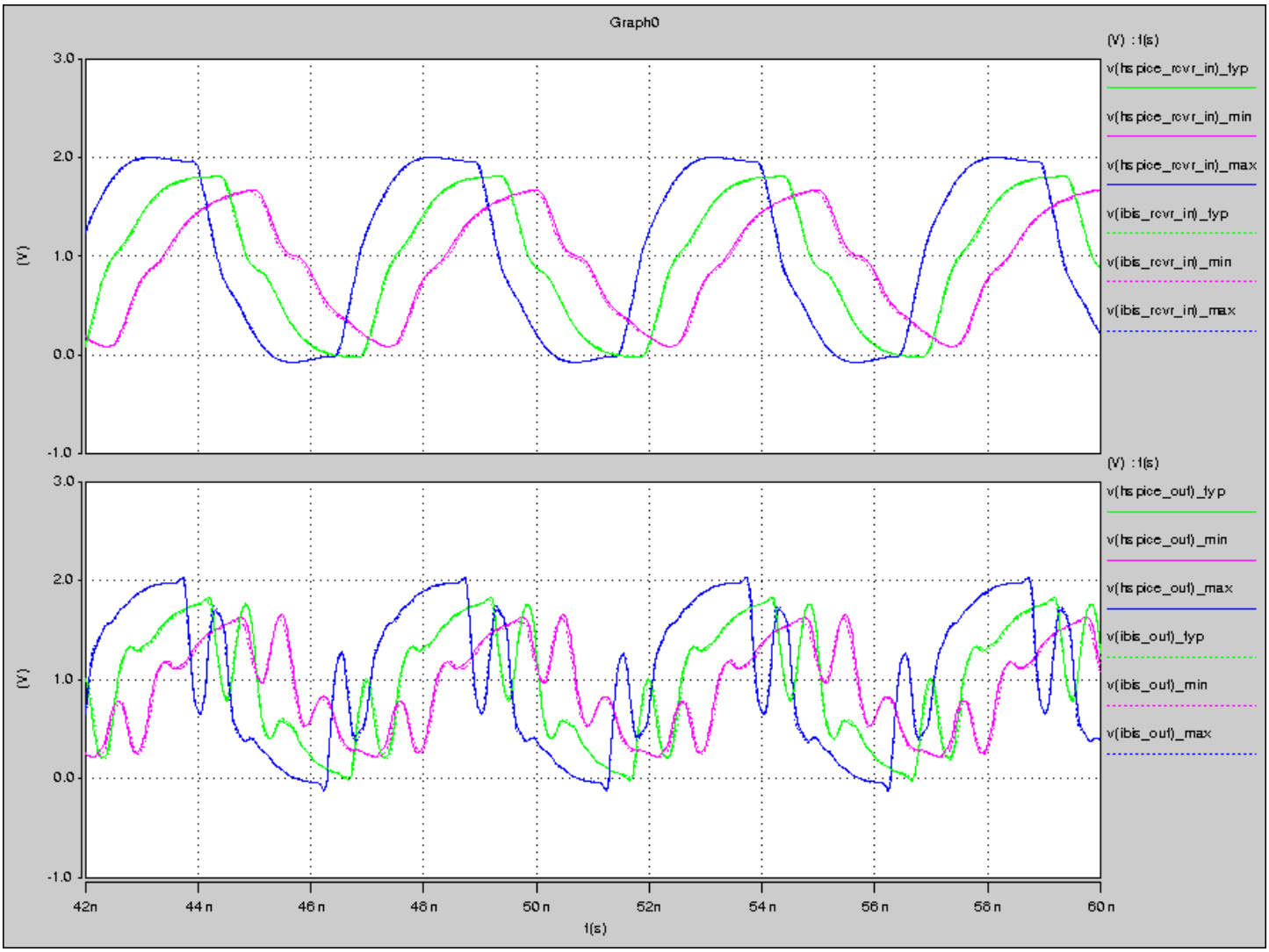
IBIS vs HSPICE Correlation

1. ☒ For all output model or I/O model run hspice transient simulation using encrypted netlist and using IBIS model (b-element).
   a. ☒ Use the below setup and node naming conventions for the IBIS and HSPICE deck file (.sp file). Indicate and update the setup diagram if it is different. Indicate version of HSPICE simulator used for simulation: **2008.09**
   b. ☒ Run simulation for all corners cases and at maximum allowable speed grade

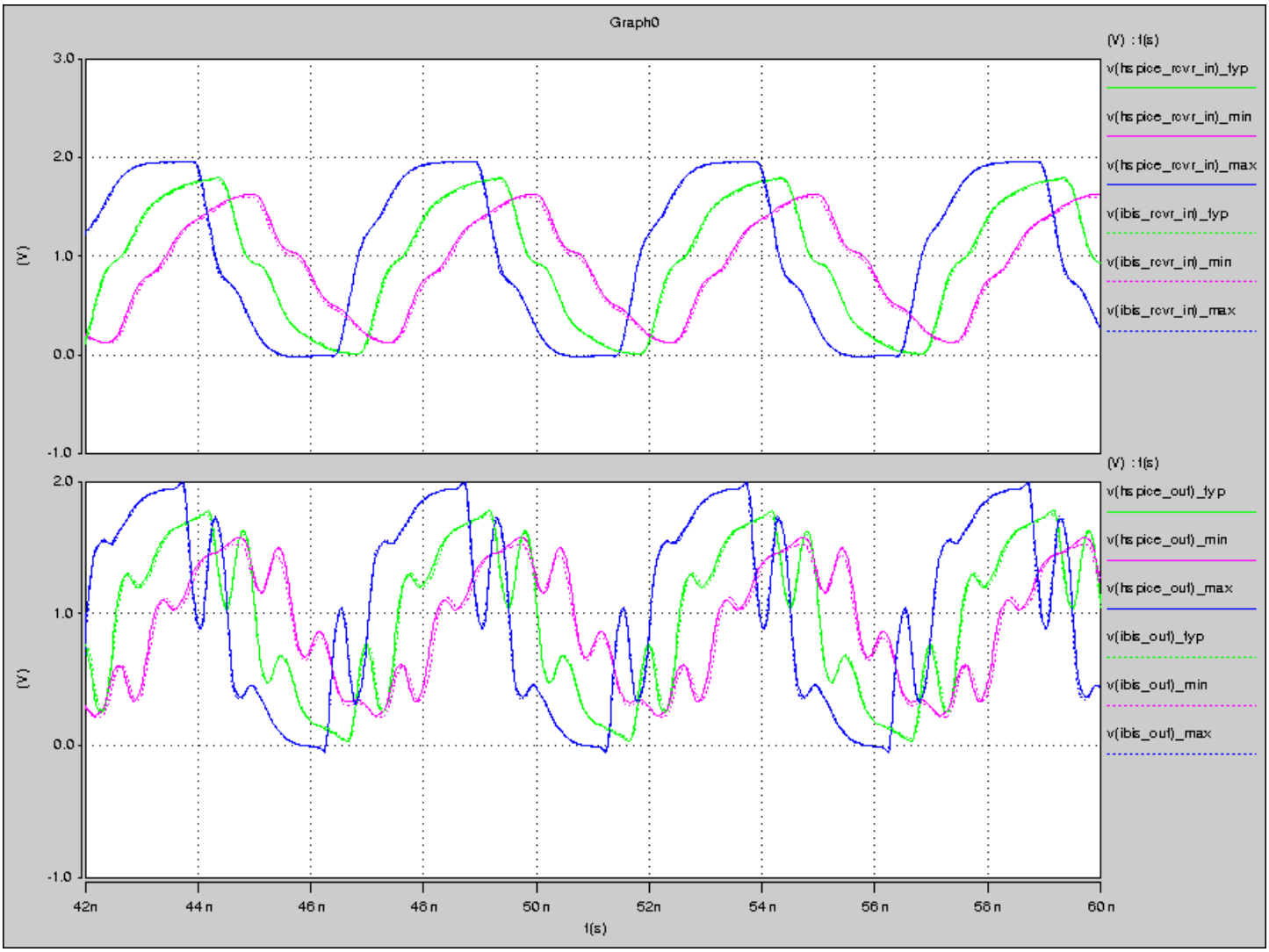
i. DQ_FULL_18 driving 20pF load



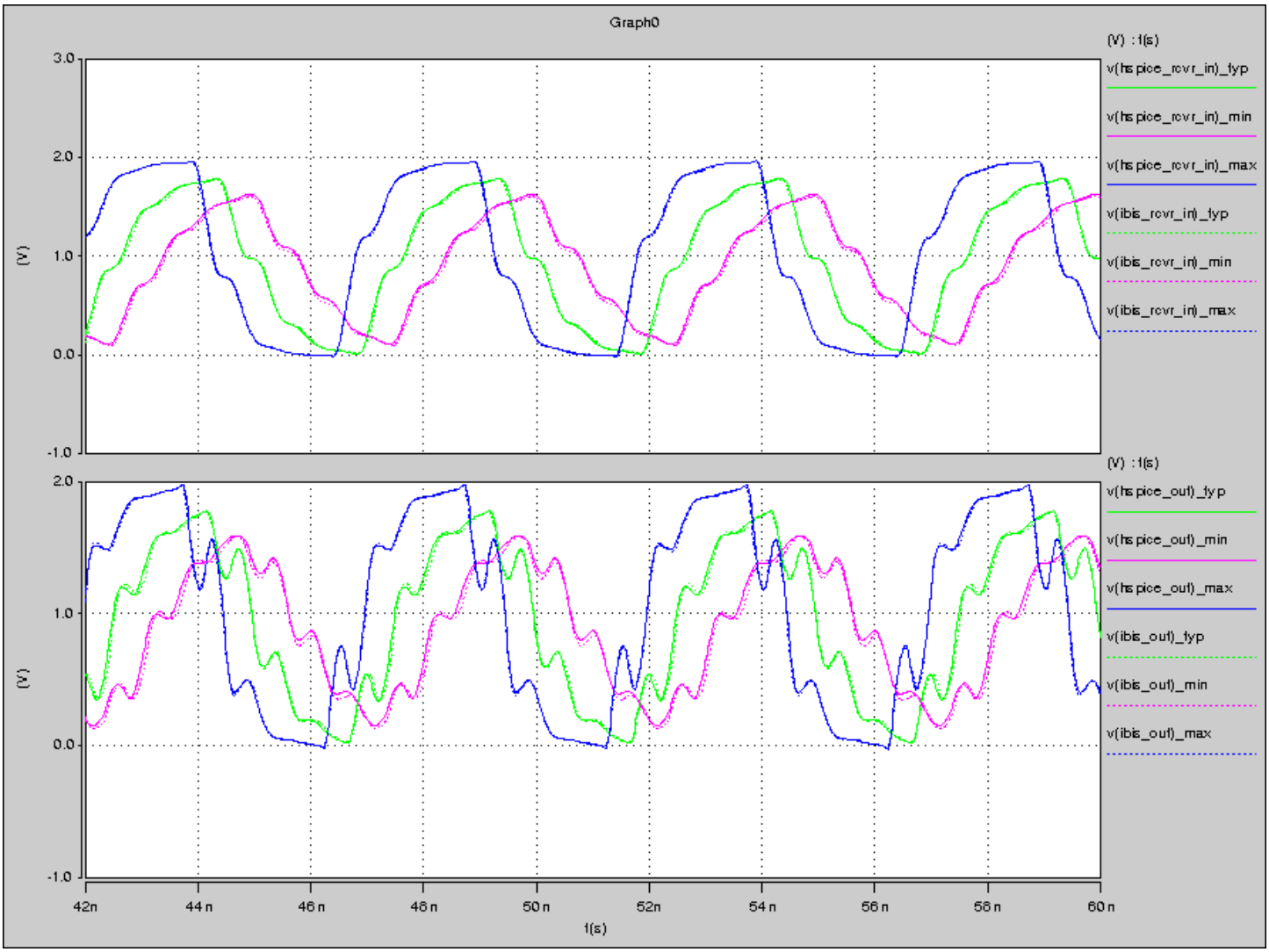
ii. DQ_3QTR_18 driving 15pF load



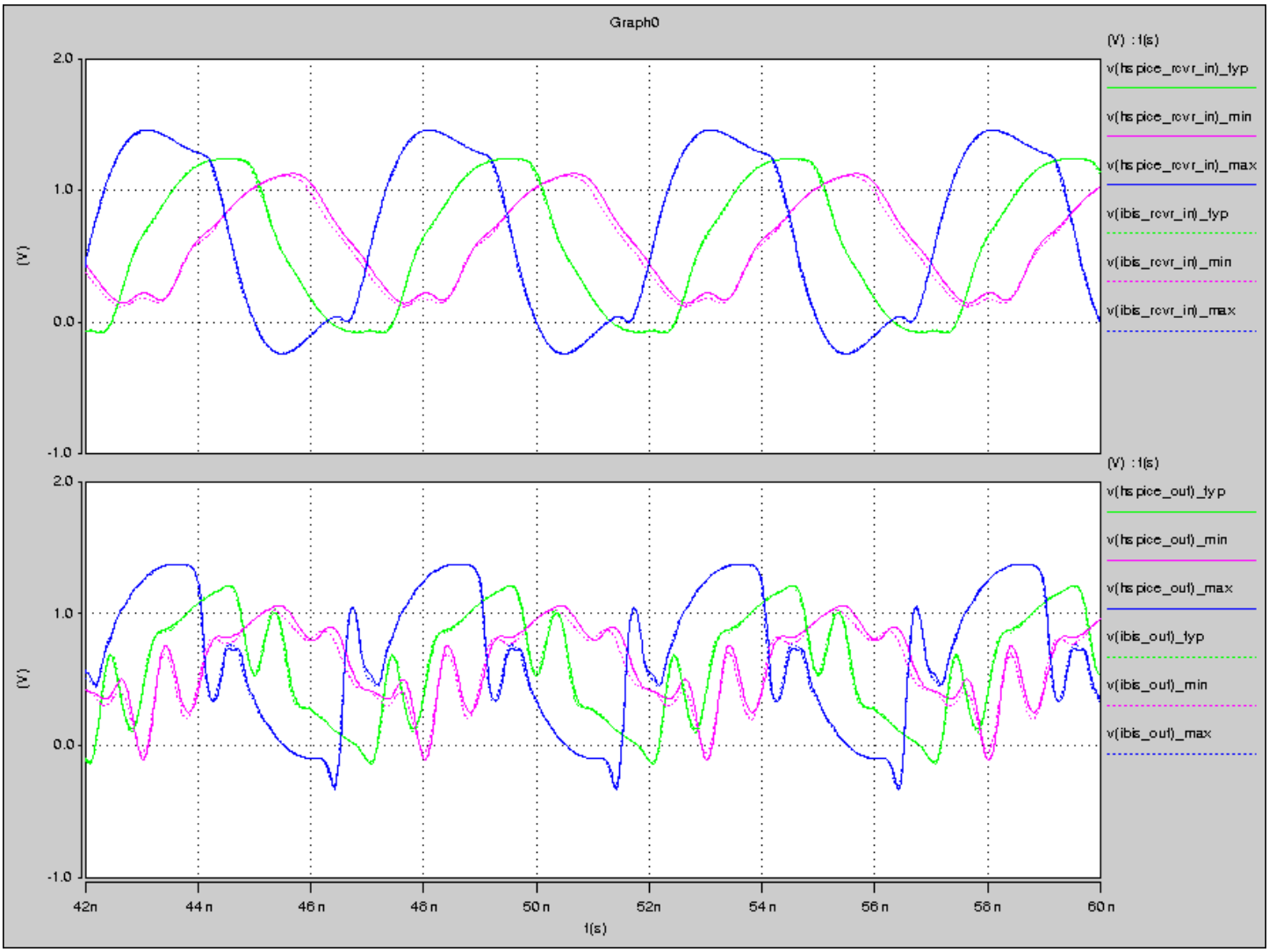
iii. DQ_HALF_18 driving 10pF load



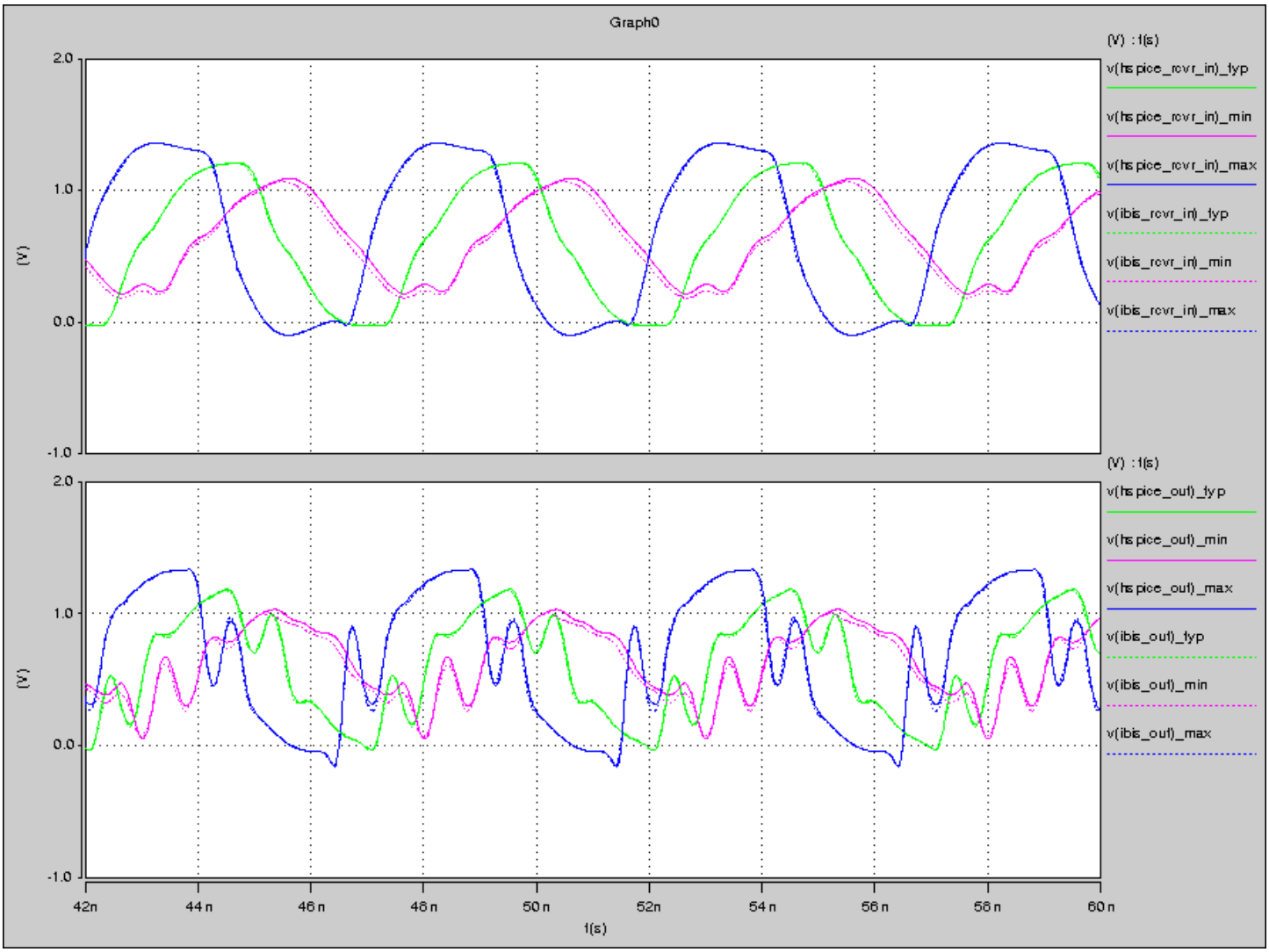
iv. DQ_QTR_18 driving 5pF load



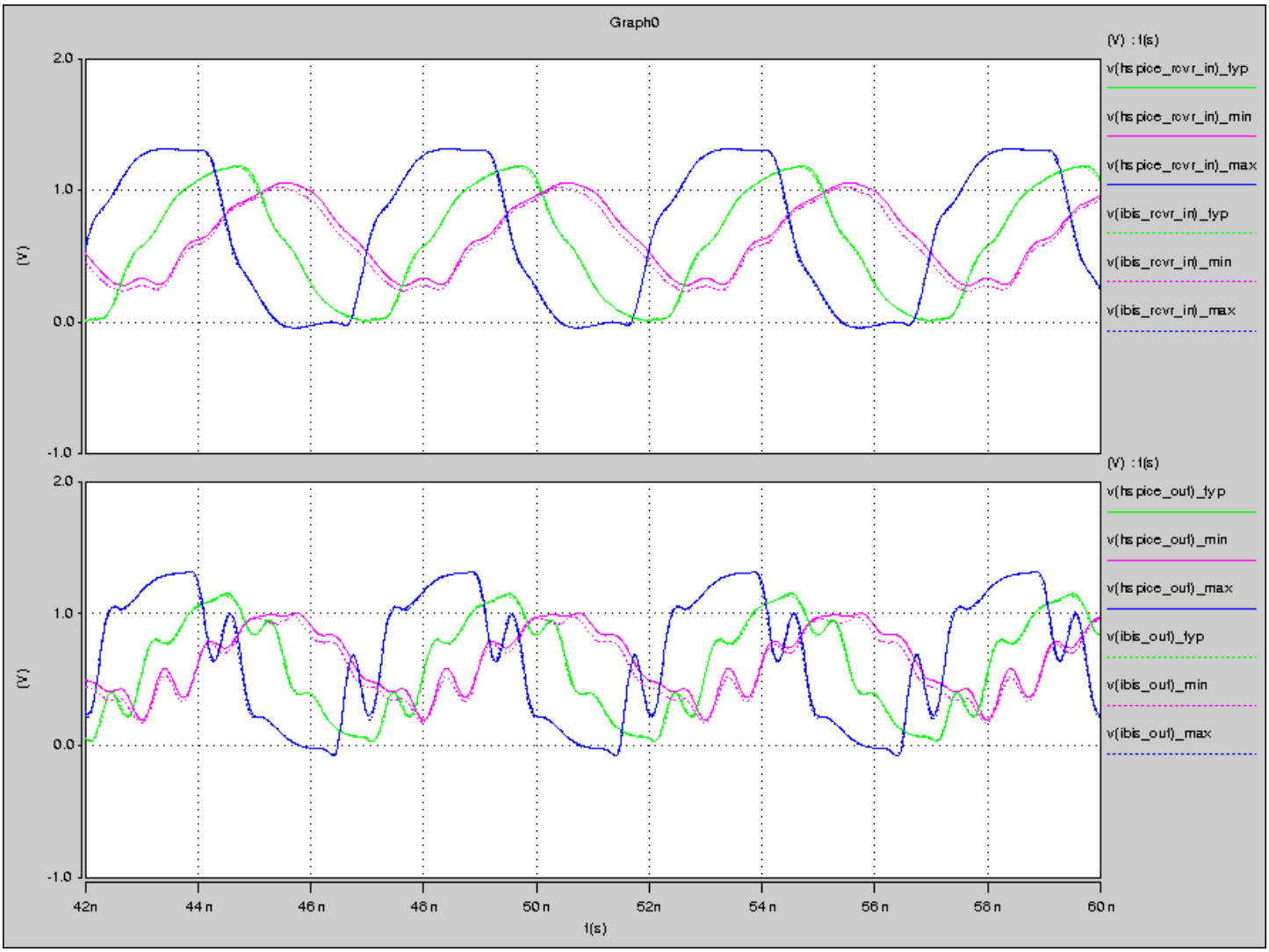
v. DQ_FULL_12 driving 20pF load



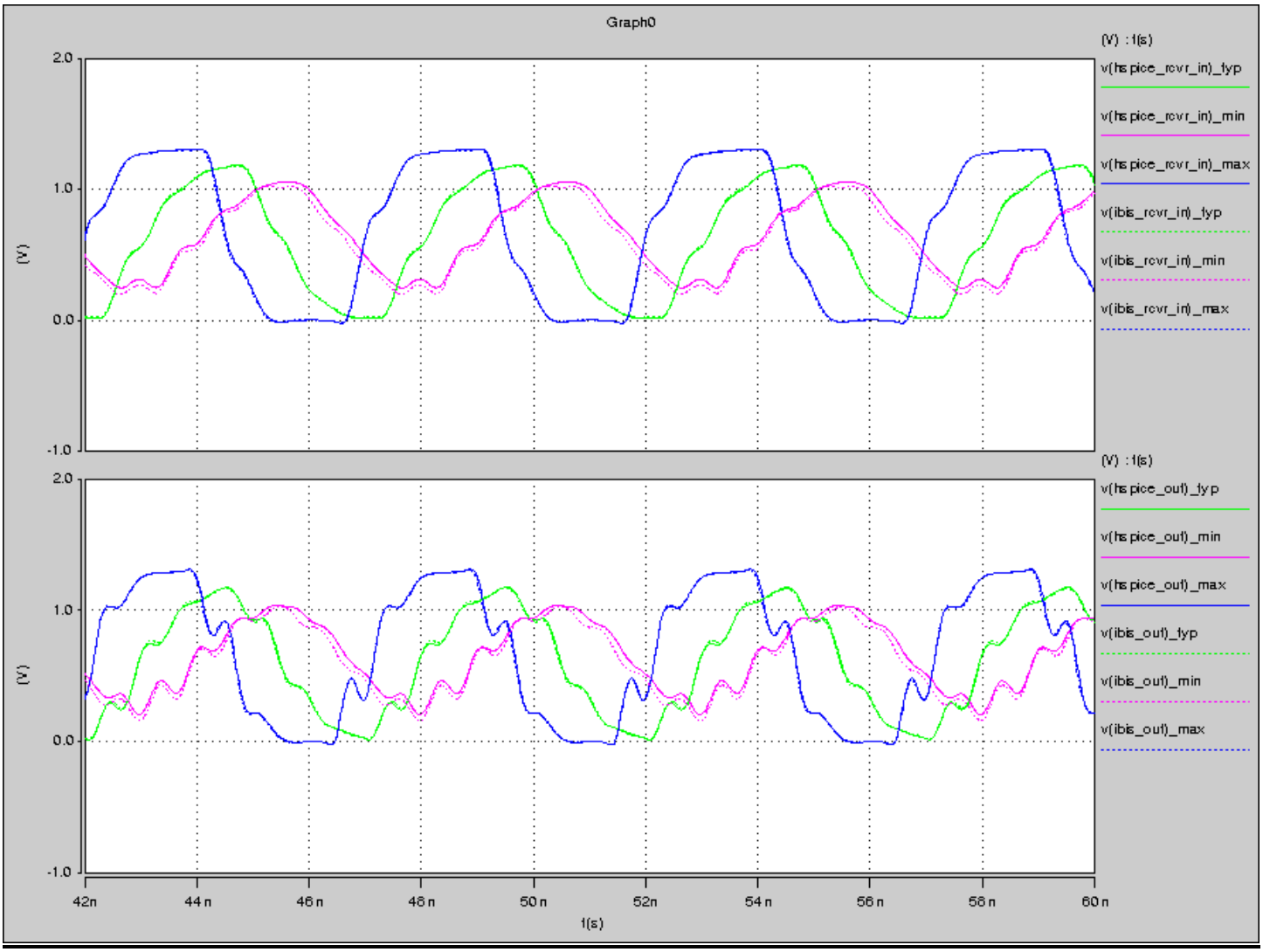
vi. DQ_3QTR_12 driving 15pF load



vii. DQ_HALF_12 driving 10pF load

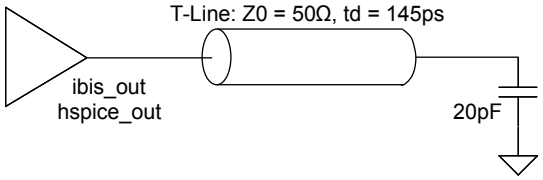


viii. DQ_QTR_12 driving 5pF load

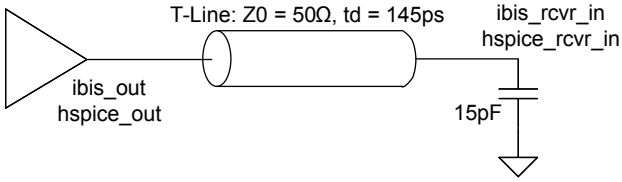


Setup

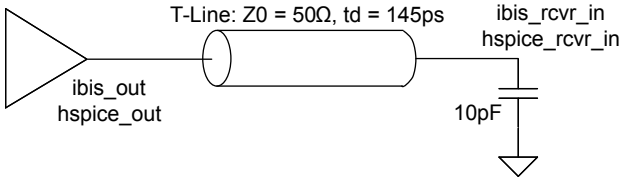
DQ_FULL_18/DQ_FULL_12



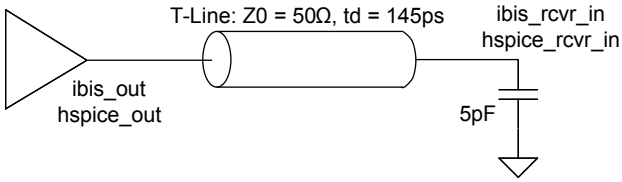
DQ_3QTR_18/DQ_3QTR_12



DQ_HALF_18/DQ_HALF_12



DQ_QTR_18/DQ_QTR_12



Comments

1. The Model does not reflect actual part number availability.
2. Datasheet capacitance values are preliminary.

Document Revision History

Rev **1.0** – **06/16/2009**

a. IBIS revision **1.0**
b. HSPICE revision **1.0**

Rev **2.0** – **02/15/2010**

a. IBIS revision **2.0**
b. HSPICE revision **2.0**

